

What is claimed is:

Sub.
A1

1 1. A method comprising:
2 initializing a circuit said circuit having at least one memory element coupled to
3 a memory bus on a host system;
4 monitoring signals on the memory bus;
5 detecting a first sequence of signals; and
6 switching control of the at least one memory element to the circuit.

1 2. The method of claim 1 further comprising:
2 detecting a second sequence of signals; and
3 switching control of the at least one memory element to the host system

1 3. The method of claim 2 wherein error correcting codes are switched off prior to
2 switching control of the at least one memory element to the host system.

1 4. The method of claim 1 wherein initializing a circuit having at least one memory
2 element coupled to a memory bus on a host system comprises detecting a sequence of
3 writes to memory locations on the circuit.

1 5. The method of claim 4 wherein the sequence of writes are writes to random
2 memory locations on the circuit.

1 6. The method of claim 1 wherein monitoring signals on the memory bus
2 comprises the circuit monitoring control, address, and data signals on the host system.

09965387-092701

Sub
A1

09965387, 092701

- 1 7. The method of claim 1 wherein detecting a first sequence of signals comprises
2 detecting at least one write signal to a particular memory location on the circuit.
- 1 8. The method of claim 1 wherein detecting a first sequence of signals comprises
2 detecting at least one read signal from a particular memory location on the circuit.
- 1 9. The method of claim 1 wherein switching control of the memory bus to the
2 circuit comprises a processing element in the circuit reading from or writing to the
3 memory in the circuit.
- 1 10. The method of claim 2 wherein switching control of the at least one memory
2 element to the host system comprises a processor on the host system reading from or
3 writing to the at least one memory element.
- 1 11. An apparatus comprising:
2 a memory bus on a host system;
3 a plurality of memory elements on a circuit, said plurality of memory elements
4 communicatively coupled with the memory bus;
5 a processing element on the circuit communicatively coupled with the plurality
6 of memory element and the memory bus, said processing element to
7 monitor signals on the memory bus;
8 detect a first sequence of signals; and
9 switch control of the plurality of memory elements to the circuit.

09965387-092701
10/22/00 18:59:56

Sub
A1

1 12. The apparatus of claim 11 further comprising said processing element to detect
2 a second sequence of signals; and
3 switch control of the plurality of memory elements to the host system.

1 13. The apparatus of claim 12 wherein error correcting codes are switched off prior
2 to switching control of the plurality of memory element to the host system.

1 14. The apparatus of claim 11 wherein the processing element is at least one of a
2 field programmable gate array, and a processor.

1 15. The apparatus of claim 11 wherein the processing element to monitor signals on
2 the memory bus comprises the processing element to monitor control, address, and data
3 signals on the host system.

1 16. The apparatus of claim 11 wherein the processing element to detect a first
2 sequence of signals comprises the processing element to detect at least one write signal
3 to a particular memory element on the circuit.

1 17. The apparatus of claim 11 wherein the processing element to detect a first
2 sequence of signals comprises the processing element to detect at least one read signal
3 to a particular memory element on the circuit.

1 18. The apparatus of claim 11 wherein the processing element to switch control of
2 the plurality of memory element to the circuit comprises the processing element reading
3 from or writing to the plurality of memory elements.

Sub
A1

09965387-092701

1 19. The apparatus of claim 12 wherein the processing element to switch control of
2 the plurality of memory elements to the circuit comprises a processor on the host
3 system reading from or writing to the plurality of memory elements.

1 20. An article of manufacture comprising:
2 a machine-accessible medium including instructions that, when executed by a
3 machine, causes the machine to perform operations comprising
4 initializing a circuit said circuit having at least one memory element coupled to
5 a memory bus on a host system;
6 monitoring signals on the memory bus;
7 detecting a first sequence of signals; and
8 switching control of the at least one memory element to the circuit.

1 21. The article of manufacture as in claim 20, further comprising instructions for
2 detecting a second sequence of signals; and
3 switching control of the at least one memory element to the host system.

1 22. The article of manufacture as in claim 21, further comprising instructions for
2 switching of error correcting codes prior to switching control of the at least one
3 memory element to the host system.

1 23. The article of manufacture as in claim 20, wherein said instructions for
2 initializing a circuit having at least one memory element coupled to a memory bus on a
3 host system comprises further instructions for detecting a sequence of writes to memory
4 locations on the circuit.

Sub
A1

1 24. The article of manufacture as in claim 23, wherein said instructions for
2 detecting a sequence of writes include further instructions for writing to random
3 memory locations on a circuit.

1 25. The article of manufacture as in claim 20, wherein said instructions for
2 monitoring signals on the memory bus comprises further instructions for the circuit
3 monitoring control, address, and data signals on the host system.

1 26. The article of manufacture as in claim 20, wherein said instructions for
2 detecting a first sequence of signals comprises further instructions for detecting at least
3 one write signal to a particular memory location on the circuit.

1 27. The article of manufacture as in claim 20, wherein said instructions for
2 detecting a first sequence of signals comprises further instructions for detecting at least
3 one read signal from a particular memory location on the circuit.

1 28. The article of manufacture as in claim 20, wherein said instructions for
2 switching control of the memory bus to the circuit comprises further instructions for a
3 processing element in the circuit reading from or writing to the memory in the circuit.

1 29. The article of manufacture as in claim 21, wherein said instructions for
2 switching control of the at least one memory element to the host system comprises
3 further instructions for a processor on the host system reading from or writing to the at
4 least one memory element.

09965387-092701